IN THE CLAIMS

1. (currently amended) A processing system comprising:

a processor;

a volatile memory device coupled to communicate with the processor; and

a non-volatile memory device coupled to the processor and connected to the volatile memory device, wherein the non-volatile memory device transfers data directly to the volatile memory device during power-up without intervention by any other device ~~control from the processor~~.

2. (original) The processing system of claim 1 wherein the volatile memory device initiates the data transfer in response to a reset signal.

3. (original) The processing system of claim 1 wherein the volatile memory device provides a system reset signal to the processor after the data is transferred from the non-volatile memory device.

4. (original) The processing system of claim 1 wherein the processor is coupled to store data in the non-volatile memory device via a serial bus.

5. (original) The processing system of claim 1 wherein the volatile memory device initiates the data transfer in response to a reset signal provided by an external reset controller.

6. (currently amended) A processing system comprising:

a processor;

a synchronous memory device coupled to communicate with the processor via a synchronous bus; and

a flash memory device coupled to communicate with the processor via a serial bus and connected to the synchronous memory device via a dedicated direct bus, wherein the flash memory device transfers data directly to the synchronous memory device during power-up without intervention by any other device.

7. (original) The processing system of claim 6 wherein the synchronous memory device initiates the data transfer in response to a reset signal provided by an external reset controller.

8. (original) The processing system of claim 7 wherein the synchronous memory device provides a system reset signal to the processor after the data is transferred from the flash memory device.

9. (original) The processing system of claim 6 wherein the synchronous memory device is an SDRAM.

10. (original) The processing system of claim 6 wherein the synchronous memory device is an RDRAM.

11. (currently amended) A processor system power-up method comprising:

detecting a power-up condition and providing a reset signal to a synchronous memory;

initiating a direct data transfer from a non-volatile memory to the synchronous memory, without intervention from any other device, in response to the reset signal; and

providing a system reset signal from the synchronous memory to a processor upon completion of the direct data transfer.

12. (previously presented) The method of claim 11 wherein the synchronous memory device is an SDRAM.

13. (previously presented) The method of claim 11 wherein the synchronous memory device is an RDRAM.

14. (original) The method of claim 11 wherein the non-volatile memory is flash memory.

15. (original) The method of claim 11 further comprises loading the non-volatile memory with the processor prior to detecting the power-up condition.

16. (currently amended) A method of improving a processor system power-up comprising:

detecting a power-up condition with a reset controller and providing a reset signal to a synchronous memory;

using the synchronous memory, initiating a direct data transfer from a flash memory to the synchronous memory, over a dedicated bus and without intervention, in response to the reset signal; and

providing a system reset signal from the synchronous memory to a processor after the data has been transferred.

17. (original) The method of claim 16 wherein the synchronous memory is coupled to the processor via a synchronous bus.

18. (previously presented) The method of claim 16 wherein the synchronous memory device is either an SDRAM or an RDRAM.

19. (currently amended) A method of increasing a processor system power-up speed comprising:

detecting a power-up condition with a reset controller and providing a reset signal to a synchronous dynamic random access memory (SDRAM);

using the SDRAM, initiating a direct data transfer from a flash memory to the synchronous memory, over a dedicated bus and without intervention, in response to the reset signal; and

providing a system reset signal from the SDRAM to a processor after the data has been transferred.

20. (currently amended) A processor system power-up method comprising:

detecting a power-up condition with a reset controller and providing a reset signal to a rambus dynamic random access memory (RDRAM);

using the RDRAM, initiating a direct data transfer from a flash memory to the synchronous memory, over a dedicated bus and without intervention, in response to the reset signal; and

providing a system reset signal from the RDRAM to a processor after the data has been transferred.

21. (currently amended) A data transfer method comprising:

initiating a direct data transfer from a non-volatile memory to a volatile storage device; and

transferring data from the non-volatile memory to the volatile storage device without intervention from any other device ~~control from an external processor~~.